AMENDMENTS

In The Specification:

In accordance with Rule § 1.121 , please amend the specification by substituting the following replacement paragraph. All deleted material is shown by strike-through effects. All added text is underlined. No new matter is added by the amendments listed below:

Page 4, lines 22-23:

The present invention will be described in more detail with reference to the ~~accompanied~~ following drawings.

Page 6, lines 20-22:

Fig. 2 is a timing diagram illustrating entry and exit ~~operation~~ operations of the self-refresh device in a PASR operation according to the present invention.

Page 12, lines 15-18:

When the EMRS code is "QUARTER ARRAY", the PASR decoder 40 activates the control signal PASR_BK0, and inactivates the control signals PASR_BK1 and PSR_BK23. As a result, the RAS generator 50 ~~is maintained at an active~~ remains activated.

Page 14, lines 16-19:

For example the self-refresh device refreshes [[8K]] 8000 times for ~~64msec~~ 64 ms, the refresh request signal REF_RQ generates [[8K]] 8000 pulse signals for ~~64msec~~ 64 ms and a time interval between pulses becomes [[8usec]] 8 μs.

Page 18, lines 10-16

The inverter IV8 outputs a register set address bit EMRSAZ<0> by inverting the register set address bit EMRSA<0>. The inverter IV9 outputs a register set address bit EMRSAZ<1> by inverting the register set address bit EMRSA<1>. The inverter IV10 outputs a register set ~~addressbit~~ address bit EMRSAZ<2> by inverting the register set address bit EMRSA<2>.

Page 22, lines 2-4:

Here, the NMOS transistor N3 has a gate to receive the refresh operation signal R_ACT, and the NMOS transistor N4 has a gate to receive the control signal PASR_BK<j>.